REMARKS

Claims 1-47 are pending in the present application. By this amendment, claims 1-4. 7, 15-16, and 19-20 have been amended to improve formal structure and not to overcome a rejection based on cited art. No new matter has been added. Accordingly, claims 1-47 are currently under consideration. Applicant respectfully submits that these claims are allowable.

Claim Rejections Under 35 USC § 102

Claims 1-8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Agrawal et al. (U.S. Patent No. 5,490,074). Applicant respectfully submits that the claims, as amended are allowable over the cited references and all references of record.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. (MPEP 2131)

Claim 1 defines *"Within a programmable logic device, a routing architecture to interconnect a plurality of function blocks."* Agrawal et al. does not disclose a *"an electrically optimum physical length"* as claimed by claim 1.

It is well-settled that an Applicant may be his or her own lexicographer. "Where an explicit definition is provided by the applicant for a term, that definition will control interpretation of the term as used in the claim." (MPEP 2111.01 (III)) In this case the Applicant has identified electrical optimality with speed optimality both in the original specification (e.g., page 4, lines 5-7) and in subsequent remarks (Reply filed April 15, 2004, pp. 18-19) so as to provide an explicit definition for *"electrically optimum."* As noted above, this definition must control the interpretation of the claim. Agrawal et al. simply does not disclose *"an electrically optimum physical length"* as claimed by claim 1.

The Examiner has cited col. 6, lines 45-50, of Agrawal et al. for an architecture that "supports efficient utilization of the resources ... without speed penalty" and conflated this with

"electrically optimum" as claimed by claim 1. However, this reference to Agrawal et al. is taken from a context related to the analysis of a logic block architecture where the words "without speed penalty" cannot be identified with *"electrically optimum"* as claimed by claim 1. The portion of Agrawal et al. cited by the Examiner is further developed later in the patent. FIG. 27 shows "a schematic diagram of the combinatorial logic in the configuration logic block" (col. 8, lines 11-12.) A discussion of FIG 27 begins on at col. 21, line 35, and continues with reference to subsequent figures on various multiplexing options for the logic block. At col. 26, lines 55-62, we have:

> "Thus, the configurable logic block described above provides for symmetrical interfaces on all four sides of the block to the interconnect structure. Furthermore, it allows for wide gating and narrow gating functions without suffering a speed penalty for the narrow gated functions. Furthermore, the wide gating functions do not require sharing of input signals which complicates logic design using the configuration logic block." (emphasis added.)

Thus, this reference to a "speed penalty" is taken from the context of gating functions in a logic architecture and cannot be identified with *"electrically optimum"* as claimed by claim 1.

Further, the Examiner has cited portions of Agrawal et al. that are not applicable to a *"routing architecture"* as claimed by claim 1. "Any terminology in the preamble that limits the structure of the claimed invention must be treated as a claim limitation." (MPEP 2111.02) With respect to the above-cited rejection, the Examiner has cited portions of the reference that relate a logic architecture, not a *"routing architecture"* as claimed by claim 1. For example, the Examiner cites col. 6, lines 45-50, which refer to a "configurable logic block architecture." The Examiner cannot properly read this disclosure as applying to a *"routing architecture"* as claimed by claim 1.

The above-cited characteristic features of the present invention, defined clearly in claim 1 of the present invention, are not disclosed or suggested by the cited reference. Therefore, claim 1 is allowable over the cited reference. Because they depend directly or indirectly from claim 1, claims 2-8 are likewise allowable over the cited reference.

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Applicant respectfully requests that the above-cited rejection under 35 U.S.C. § 102(b) be withdrawn.

Claim Rejections Under 35 USC § 103

Claims 9-17 and 19-23 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Agrawal et al. (U.S. Patent No. 5,490,074) and further in view of Young (U.S. Patent No. 5,818,730). Applicant respectfully submits that the claims, as amended are allowable over the cited references and all references of record.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to on of ordinary skill in the art, to modify the reference or to combine teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (M.P.E.P. 2143)

Claim 9 defines *"Within a programmable logic device, a two dimensional routing architecture to interconnect a plurality of function blocks."* As discussed above with respect to claim 1, the Examiner cannot ignore Applicant's definition of *"electrically optimum"*, so that Agrawal et al. does not disclose *"an electrically optimum physical length"* as claimed by claim 9. Further, the Examiner cannot properly read the cited portions of Agrawal et al. to apply to a *"routing architecture"* as claimed by claim 9

Likewise Young does not disclose *"an electrically optimum physical length"* as claimed by claim 9. Young's relevant focus is outlined in the Background section: "To minimize cost, surface area must be used efficiently, particularly where a relatively large number of signal paths must be provided within a relatively small surface area. Therefore, there is a need to use a shared diffusion area which maximizes the number of paths for the diffusion area or, alternatively, minimizes the diffusion area for a given number of paths." (col. 1, lines 39-45.) Young's solution approach is then outlined in Summary of the Invention: "A structure and method are provided for

designing the wiring layout or routing paths in a programmable logic integrated circuit device for maximizing the number of paths for an available diffusion area or, alternatively, for minimizing the required diffusion area for a given number of paths." (col. 1, lines 47-52.) Young's focus on shared diffusion as a characteristic of efficiency simply has nothing to do with *"an electrically optimum physical length"* as claimed by claim 9.

The Examiner has cited Young at col. 1, lines 39-52, but this discussion on shared diffusion says nothing about speed optimality and thereby teaches away from the present invention. Similarly the Examiner has cited col. 5, lines 18-35, where again efficiency is discussed without reference to speed optimality. Note however that although Young is focused on shared diffusion he mentions speed improvement (not optimality) as a secondary effect of the disclosed structures at col. 4, lines 63-65. This improvement results from the overall layout (i.e., shared diffusion) and not an optimization of wire length for speed optimality. In this way also, Young teaches away from the present invention.

The above-cited characteristic features of the present invention, defined clearly in claim 9 of the present invention, are not disclosed or suggested by the cited references. Therefore, claim 9 is allowable over the cited references. Because they depend directly or indirectly from claim 9, claims 10-14 are likewise allowable over the cited references.

Claim 15 defines a *"method to interconnect a plurality of function blocks within a programmable logic device."* As discussed above with respect to claim 9, the Examiner cannot ignore Applicant's definition of *"electrically optimum"*, and so neither Agrawal et al. nor Young discloses *"a physical length that is electrically optimum for a wire"* as claimed by claim 15. Therefore, claim 15 is allowable over the cited references. Because they depend directly or indirectly from claim 15, claims 16-19 are likewise allowable over the cited references.

Claim 20 defines a *"Within a programmable logic device, a two-dimensional routing architecture to interconnect a plurality of function blocks."* As discussed above with respect to claim 9, the Examiner cannot ignore Applicant's definition of *"electrically optimum"*, and so

neither Agrawal et al. nor Young discloses *"an electrically optimum physical length"* as claimed by claim 20. Further, the Examiner cannot properly read the cited portions of Agrawal et al. to apply to a *"routing architecture"* as claimed by claim 20. Therefore, claim 20 is allowable over the cited references. Because they depend directly or indirectly from claim 20, claims 21-23 are likewise allowable over the cited references.

Applicant respectfully requests that the above-cited rejection under 35 U.S.C. § 103 be withdrawn.

Allowable Subject Matter

Claims 24-44 stand allowed. Applicant respectfully requests that claims 45-47 be allowed, since they depend from allowed claims.

Claim 18 stands objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. As discussed above, claim 18 is allowable.

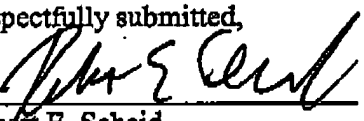
CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. **03-1952** referencing docket no. **306812002500**. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: September 24, 2004

Respectfully submitted,

By 

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